

U.S. Department of Commerce, Patent and Trademark				Atty. Docket No.		Application No.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				SNDK.327US0		10/774,014	
(Use several sheets if necessary)				Applicants		Conf. No.	
(Form PTO-1449)				Gerrit Jan HEMINK		8419	
Filing Date				February 6, 2004		Art Group	
February 6, 2004						2827	

  

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 PATENT & TRADEMARK OFFICE

**U.S. Patent Documents**

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
MT	1	5,677,873	10-1997	Choi et al.		/
	2	5,793,677	08-1998	Hu et al.		
	3	5,969,985	10-1999	Tanaka et al.		
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	5	6,044,013	03-2000	Tanaka et al.		
	6	6,061,270	05-2000	Choi		
	7	6,154,391	11-2000	Takeuchi et al.		
	8	6,282,117 B1	08-2001	Tanaka et al.		
	9	6,363,010 B2	03-2002	Tanaka et al.		
	10	6,493,265 B2	12-2002	Satoh et al.		
	11	6,545,909 B2	04-2003	Tanaka et al.		
	12	6,717,861 B2	04-2004	Jeong et al.		
	13	6,859,394 B2	02-2005	Matsunaga et al.		
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MT	15	6,930,921 B2	08-2005	Matsunaga et al.		

  

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MT	16	2005/0047210 A1	03-2005	Matsunaga et al.		/
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MT	18	2005/0226055 A1	10-2005	Guterman		

  

**OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)**

Examiner	/Michael Tran/	Date Considered	07/07/2006
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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MT	19	Choi et al., "A Novel Booster Plate Technology in High Density NAND Flash Memories for Voltage Scaling Down and Zero Program Disturbance", 1996 Symposium on VLSI Technology Digest of Technical Papers, 0-7803-3342-X/96/IEEE, 4 pages.	
	20	Kim et al., "Fast Parallel Programming of Multi-Level NAND Flash Memory Cells Using the Booster-Line Technology", Symposium on VLSI Technology Digest of Technical Papers, (1997), 2 pages.	
	21	Brown et al., Editors, "Nonvolatile Semiconductor Memory Technology, A Comprehensive Guide to Understanding and Using NVSM Devices", IEEE Press Series on Microelectronic Systems, (1998), 57 pages.	
	22	Cho et al., "A Dual Mode NAND Flash Memory: 1-Gb Multilevel and High-Performance 512-Mb Single-Level Modes", IEEE Journal of Solid-State Circuits, Vol. 36, No. 11, Nov. 2001, 9 pages.	
	23	Satoh et al., "A Novel Gate-Offset NAND Cell (GOC-NAND) Technology Suitable for High-Density and Low-Voltage Operation Flash Memories", IEDM Technical Digest, Dec. 1999, 6 pages.	
MT	24	Jung et al., "A 3.3-V Single Power Supply 16-Mb Nonvolatile Virtual DRAM Using a NAND Flash Memory Technology", IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, Nov. 1997, 12 pages.	
Examiner /Michael Tran/		Date Considered 07/07/2006	
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							Translation	
		Document	Date	Country	Class	Subclass	Yes	No

  

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	13	K. D. Suh et al. in "A 3.3 V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme," Journal of Solid-State Circuits, Vol 30, No. 11, Nov. 1995, pp. 1149-55.
MT	14	T. S. Jung et al. proposed a local self boosting ("LSB") technique in "A 3.3V 128Mb Multi-Level NAND Flash Memory for Mass Storage Applications", ISSCC96, Session 2, Flash Memory, Paper TP 2.1, IEEE, pp. 32. Feb. 1996.

  

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